In the Claims:

1. (Currently Amended) A method for fabricating a transistor structure~~,~~ comprising at least a first and a second bipolar transistor having different collector widths ~~(C1, C2)~~, the method comprising:

A) providing a semiconductor substrate ~~(1) being provided~~,

B) introducing at least a first buried layer ~~(5.1)~~ of the first bipolar transistor and a second buried layer ~~(5.2)~~ of the second bipolar transistor ~~being introduced~~ into the semiconductor substrate ~~(1)~~, and

C) ~~there being produced~~producing at least a first collector region ~~(2.1)~~ having a first collector width ~~(C1)~~ on the first buried layer ~~(5.1)~~ and a second collector region ~~(2.2)~~ having a second collector width ~~(C2)~~ on the second buried layer ~~(5.2)~~,

wherein

a) for the production of the second collector width ~~(C2)~~, a first collector zone ~~(2.2.1)~~ having a first thickness ~~(C3)~~ is produced on the second buried layer, ~~(5.2) and~~

b) a second collector zone ~~(2.2.2)~~ having a second thickness ~~(C4)~~ is produced on the first collector zone ~~(2.2.1)~~, and

c) at least one insulation region ~~(4)~~ is produced~~,~~ which isolates at least the collector regions ~~(2.1, 2.2)~~ from one another.

2. (Currently Amended) A method for fabricating a transistor structure~~,~~ comprising at least a first and a second bipolar transistor having different collector widths ~~(C1, C2)~~, the method comprising:

A) providing a semiconductor substrate ~~(1) being provided~~, and

B) ~~there being produced~~producing at least a first collector region ~~(2.1)~~ of the first bipolar transistor having a first collector width ~~(C1)~~ and a second collector region ~~(2.2)~~ of the second bipolar transistor having a second collector width ~~(C2)~~,

wherein

a) at least a first zone ~~(5.1.1)~~ of a first buried layer ~~(5.1)~~ of a first conductivity type of the first bipolar transistor and a first zone ~~(5.2.1)~~ of a second buried layer ~~(5.2)~~ of a first or a second conductivity type of the

second bipolar transistor are introduced into the semiconductor substrate ~~(1)~~,

b) a first epitaxial layer ~~(9)~~ is produced, which covers, over the whole area, at least the first zones ~~(5.1.1, 5.2.1)~~,

c) at least a second zone ~~(5.1.2)~~ of the first conductivity type is produced within the first epitaxial layer ~~(9)~~, the second zone ~~(5.1.2)~~ adjoining the first zone ~~(5.1.1)~~ of the first buried layer ~~(5.1)~~,

d) a second epitaxial layer ~~(10)~~ is produced, which covers, over the whole area, at least the first epitaxial layer ~~(9)~~ and the second zone ~~(5.1.2)~~ of the first buried layer ~~(5.1)~~,

d) at least one insulation region ~~(4)~~ is produced~~,~~ which isolates at least the collector regions ~~(2.1, 2.2)~~ from one another, and

e) the second zone ~~(5.1.2)~~ of the first buried layer ~~(5.1)~~ ~~adjoining~~ adjoins the first collector region ~~(2.1)~~ and the first zone ~~(5.2.1)~~ of the second buried layer ~~(5.2)~~ ~~adjoining~~ adjoins the second collector region ~~(2.2)~~.

3. (Currently Amended) A method for fabricating a transistor structure~~,~~ comprising at least a first and a second bipolar transistor having different collector widths ~~(C1, C2)~~, the method comprising:

A) providing a semiconductor substrate ~~(1) being provided~~, and

B) ~~there being produced~~producig at least a first collector region ~~(2.1)~~ of the first bipolar transistor having a first collector width ~~(C1)~~ and a second collector region ~~(2.2)~~ of the second bipolar transistor having a second collector width ~~(C2)~~,

wherein

a) at least a first zone ~~(5.1.1)~~ of a first buried layer ~~(5.1)~~ of a first conductivity type of the first bipolar transistor and a second buried layer ~~(5.2)~~ of a first or a second conductivity type of the second bipolar transistor are introduced into the semiconductor substrate ~~(1)~~,

b) at least a first collector zone ~~(2.1.1)~~ of the first bipolar transistor and a first collector zone ~~(2.2.1)~~ of the second bipolar transistor are produced, the first collector zone ~~(2.1.1)~~ of the first bipolar transistor

adjoining the first zone ~~(5.1.1)~~ and the first collector zone ~~(2.2.1)~~ of the second bipolar transistor adjoining the second buried layer ~~(5.2)~~,

c) the first collector zone ~~(2.1.1)~~ is formed as the first conductivity type,

d) a second collector zone ~~(2.2.2)~~ is produced on the first collector zone ~~(2.2.1)~~ of the second bipolar transistor and a second collector zone ~~(2.1.2)~~ is produced on the first collector zone ~~(2.1.1)~~ of the first bipolar transistor, and

e) at least one insulation region ~~(4)~~ is produced, which isolates at least the collector zones ~~(2.x.y)~~ from one another.

4. (Currently Amended) The method as claimed in ~~one of claims~~ claim 1 ~~to 3~~, wherein the second collector zone ~~(2.2.2)~~ is deposited.

5. (Currently Amended) The method as claimed in claim 4, wherein the second collector zone ~~(2.2.2)~~ is deposited epitaxially.

6. (Currently Amended) The method as claimed in ~~one of claims~~ claim 1 ~~to 5~~, wherein an insulating layer ~~(2)~~ is produced between the semiconductor substrate ~~(1)~~ and the buried layers ~~(5.1, 5.2)~~.

7. (Currently Amended) The method as claimed in ~~one of claims~~ claim 1 ~~to 6~~, wherein the insulation region ~~(4)~~ is produced with the aid of shallow trench isolation technology.

8. (New) The method as claimed in claim 2, wherein the second collector zone is deposited.

9. (New) The method as claimed in claim 8, wherein the second collector zone is deposited epitaxially.

10. (New) The method as claimed in claim 2, wherein an insulating layer is produced between the semiconductor substrate and the buried layers.

11. (New) The method as claimed in claim 2, wherein the insulation region is produced with the aid of shallow trench isolation technology.

12. (New) The method as claimed in claim 3, wherein the second collector zone is deposited.

13. (New) The method as claimed in claim 12, wherein the second collector zone is deposited epitaxially.

14. (New) The method as claimed in claim 3, wherein an insulating layer is produced between the semiconductor substrate and the buried layers.

15. (New) The method as claimed in claim 3, wherein the insulation region is produced with the aid of shallow trench isolation technology.